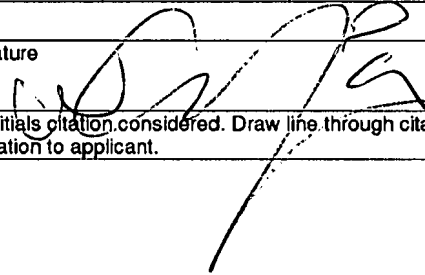
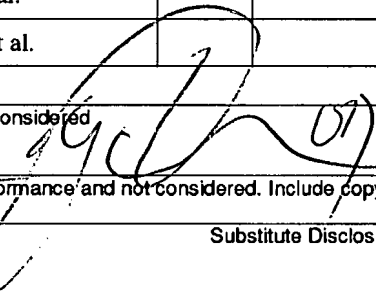


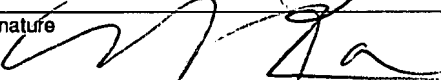
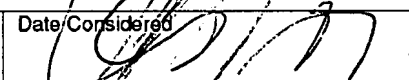
Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-306US1	Application No. 10/070,035
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date July 3, 2002	Group Art Unit 2183

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
✓	AA	2002/0038403	03/2002	Wolrich et al.			
✓	AB	3,577,189	05/1971	Cocke et al.			
✓	AC	4,471,426	09/1984	McDonough			
✓	AD	4,477,872	10/1984	Losq et al.			
✓	AE	4,569,016	02/1986	Hao et al.			
✓	AF	4,742,451	05/1988	Bruckert et al.			
✓	AG	4,755,966	07/1988	Lee et al.			
✓	AH	4,808,988	02/1989	Burke et al.			
✓	AI	4,816,913	03/1989	Harney et al.			
✓	AJ	4,847,755	07/1989	Morrison et al.			
✓	AK	4,868,735	09/1989	Moller et al.			
✓	AL	5,045,995	09/1991	Levinthal et al.			
✓	AM	5,165,025	11/1992	Lass			
✓	AN	5,170,484	12/1992	Grondalski			
✓	AO	5,187,800	02/1993	Sutherland			
✓	AP	5,189,636	02/1993	Patti et al.			
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✓	AS	5,247,671	09/1993	Adkins et al.			
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✓	AU	5,394,530	02/1995	Kitta			
✓	AV	5,428,779	06/1995	Allegrucci et al.			
✓	AW	5,463,746	10/1995	Brodnax et al.			
✓	AX	5,509,130	04/1996	Trauben et al.			
✓	AY	5,541,920	07/1996	Angle et al.			
✓	AZ	5,544,337	08/1996	Beard et al.			
✓	BA	5,572,690	11/1996	Molnar et al.			

Examiner Signature 	Date Considered 
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	


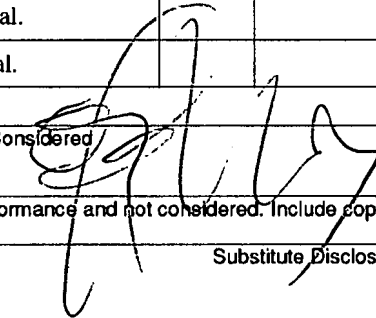
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2	BD	5,669,012	09/1997	Shimizu et al.			
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2	BY	5,944,816	08/1999	Dutton et al.			
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2	CA	5,956,514	09/1999	Wen et al.			
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5	CL	6,195,739	02/2001	Wright et al.			
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U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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W	DE	6,560,671	05/2003	Samra et al.			
W	DF	6,564,316	05/2003	Perets et al.			
W	DG	6,574,702	06/2003	Khanna et al.			
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W	DI	6,862,676	03/2005	Knapp et al.			
W	DJ	6,976,095	12/2005	Wolrich et al.			
W	DK	6,983,350	01/2006	Adiletta et al.			
W	DL	7,020,871	03/2006	Bernstein et al.			

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Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
W	DM	0 130 381	01/1985	Europe				
W	DN	0 463 855	01/1992	Europe				
W	DO	0 476 628	03/1992	Europe				
W	DP	0 696 772	02/1996	Europe				
W	DQ	WO03/019399	03/2003	WIPO				
W	DR	WO03/085517	10/2003	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
W	DS	"HART, Field Communications Protocol, Application Guide", Hart Communication Foundation, pp. 1-74, (1999).
W	DT	Bowden, Romilly, "What is HART?" Romilly's HART® and Fieldbus Web Site, 3 pages, (1997). <URL: http://www.romilly.co.uk/whathart.htm >
W	DU	Hennessy et al., <i>Computer Organization and Design: The Hardware/Software Interface</i> , Morgan Kaufman Publishers, pp. 116-119, 181-182, 225-227, 447-449, 466-470, 476-482, 510-519, 712, (1998).
W	DV	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 174-176 and 200, (1997).
W	DW	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 38-40, 143-171, and 285-288, (1997).

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Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	DX	Hidaka, Y., et al., "Multiple Threads in Cyclic Register Windows", <i>Computer Architecture News</i> , ACM, New York, NY, USA, 21(2):131-142, May 1993.
	DY	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads", <i>Proc. 19th Annual International Symposium on Computer Architecture, ACM & IEEE-CS</i> , 20(2):136-145, May 1992.
	DZ	Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, pp. 2-2, 2-3, 3-1, 7-165, C-4, and C-23, May 1999.
	EA	Jung, G., et al., "Flexible Register Window Structure for Multi-Tasking", <i>Proc. 24th Annual Hawaii International Conference on System Sciences</i> , vol. 1, pp. 110-116, (1991).
	EB	Koch, G., et al., "Breakpoints and Breakpoint Detection in Source Level Emulation", <i>Proc. 19th International Symposium on System Synthesis (ISSS '96)</i> , <i>IEEE</i> , pp. 26-31 (1996).
	EC	Moors, et al., "Cascading Content-Addressable Memories", <i>IEEE Micro</i> , 12(3):56-66 (1992).
	ED	Okamoto, K., et al., "Multithread Execution Mechanisms on RICA-1 for Massively Parallel Computation", <i>IEEE - Proc. Of PACT '96</i> , pp. 116-121 (1996).
	EE	Patterson, et al., <i>Computer Architecture A Quantitative Approach</i> , 2nd Ed., Morgan Kaufmann Publishers, Inc., pp. 447-449, (1996).
	EF	Paver, et al., "Register Locking in an Asynchronous Microprocessor", <i>IEEE</i> , pp. 351-355, (1992).
	EG	Philips ED - Philips Components: "8051 Based 8 Bit Microcontrollers, Data Handbook Integrated Circuits, Book IC20", 8051 Based 8 Bit Microcontrollers, Eindhoven, Philips, NL, pp. 5-19 (1991).
	EH	Probst et al., "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors", <i>Proceedings of the 27th Annual Hawaiian International Conference on System Sciences</i> , <i>IEEE</i> , pp. 584-593, (1994).
	EI	Quammen, D., et al., "Flexible Register Management for Sequential Programs", <i>IEEE Proc. of the Annual International Symposium on Computer Architecture</i> , Toronto, May 27-30, 1991, vol. SYMP. 18, pp. 320-329.
	EJ	Ramsey, N., "Correctness of Trap-Based Breakpoint Implementations", <i>Proc. of the 21st ACM Symposium on the Principles of Programming Languages</i> , pp. 15-24 (1994).
	EK	Steven, G.B., et al., "ALU design and processor branch architecture", <i>Microprocessing and Microprogramming</i> , 36(5):259-278, October 1993.
	EL	Young, H.C., "Code Scheduling Methods for Some Architectural Features in Pipe", <i>Microprocessing and Microprogramming</i> , Elsevier Science Publishers, Amsterdam, NL, 22(1):39-63, January 1988.
	EM	Young, H.C., "On Instruction and Data Prefetch Mechanisms", <i>International Symposium on VLSI Technology, Systems and Applications, Proc. of Technical Papers</i> , pp. 239-246, (1995).

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